

# Michael Jiayuan He

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## RESEARCH INTERESTS

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Parallel Computing, GPU Computing, Machine Learning, Placement and Routing in EDA

## EDUCATION

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**University of Texas at Austin**

**Austin, TX**

*Ph.D., Computer Science*

*Sep. 2014 – March 2022*

Advisor: *Keshav Pingali*

**Graph analytics on multicore CPUs and GPUs; Parallelization of EDA algorithms.**

***Dissertation: Detailed-routability-driven and Timing-driven Scalable Parallel Global Routing***

**Tsinghua University**

**Beijing, China**

*B.E., Microelectronics*

*Sep. 2010 – Aug. 2014*

*B.E., Economics*

## PROFESSIONAL EXPERIENCE

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**Meta Platforms (AKA Facebook)**

**Menlo Park, CA**

*Research Scientist*

*April 2022 - present*

Built state-of-the-art machine learning infrastructures for modern recommendation system (MRS), with a focus on training speedup and scalability.

**Facebook**

**Remote**

*Software Engineer Intern*

*May 2020 – Aug. 2020*

Manager: George Meng, Mentor: Lukasz Wesolowski

Performance bottleneck investigation and optimization for machine learning workloads on GPUs. Identified and optimized PyTorch performance bottlenecks; achieved significant speedup and amount of computation power savings.

**VMware**

**Palo Alto, CA**

*Research Intern*

*May 2018 – Aug. 2018*

Manager: Josh Simons, Mentor: Xin Xu

Characterization and prediction of performance interference on virtual GPUs; Investigation of P2P communication malfunction on passthrough GPU in virtual environment

## PUBLICATIONS

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- **Jiayuan He**, Udit Agarwal, Yihang Yang, Rajit Manohar, Keshav Pingali. "SPRoute 2.0: A detailed-routability-driven deterministic parallel global router with soft capacity." IEEE Asia and South Pacific Design Automation Conference (ASPDAC), 2022
- **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, and Rajit Manohar. "Interact: An Interactive Design Environment for Asynchronous Logic." Workshop on Open-Source EDA Technology (WOSET), November 2021.
- Samira Ataei, Wenmian Hua, Yihang Yang, Rajit Manohar, Yi-Shan Lu, **Jiayuan He**, Sepideh Maleki, and Keshav Pingali. "An Open-Source EDA Flow for Asynchronous Logic." IEEE Design & Test 38, no. 2 (2021): 27-37.
- Udit Agarwal, Samira Ataei, **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, Rajit Manohar. "A Digital Flow for Asynchronous VLSI Systems: Status Update." Workshop on Open-Source EDA Technology (WOSET), November 2020.
- **Jiayuan He**, Yihang Yang, Rajit Manohar. "A power router for gridded cell placement." Workshop on Open-Source EDA Technology (WOSET), November 2020.
- Yihang Yang, **Jiayuan He**, and Rajit Manohar. "Dali: A gridded cell placement flow." Workshop on Open-Source EDA Technology (WOSET), November, 2020.
- **Jiayuan He**, Martin Burtscher, Rajit Manohar, and Keshav Pingali. "SPRoute: A Scalable Parallel Negotiation-based Global Router." In 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1-8. IEEE, 2019.
- **Jiayuan He**, Martin Burtscher, Rajit Manohar, Keshav Pingali. "SPRoute: A Scalable Parallel Negotiation-based Global Router." Work-in-progress session, Design Automation Conference, June 2019.
- Xin Xu, Na Zhang, Michael Cui, **Jiayuan He**, and Ridhi Surana. "Characterization and prediction of performance interference on mediated passthrough GPUs for interference-aware scheduler." In 11th {USENIX} Workshop on Hot Topics in Cloud Computing (HotCloud 19). 2019.
- Samira Ataei, **Jiayuan He**, Wenmian Hua, Yi-Shan Lu, Sepideh Maleki, Yihang Yang, Keshav Pingali, and Rajit Manohar. "Toward a digital flow for asynchronous VLSI systems." In 2nd Workshop on Open-Source EDA Technology (WOSET), Westminster, CO, November 9, 2019.
- Yi-Shan Lu, Samira Ataei, **Jiayuan He**, Wenmian Hua, Sepideh Maleki, Yihang Yang, Martin Burtscher, Keshav Pingali, and Rajit Manohar. "Parallel Tools for Asynchronous VLSI Systems." In 1st Workshop on Open-Source EDA Technology (WOSET), San Diego, CA, November 8, 2018.
- Kuan Fang, Yufei Ni, **Jiayuan He**, Zonghui Li, Shuai Mu, and Yangdong Deng. "FastLanes: An FPGA accelerated GPU microarchitecture simulator." In Computer Design (ICCD), 2013 IEEE 31st International Conference on, pp. 241-248. IEEE, 2013. **(Best paper award)**

## **PATENTS**

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- Xin Xu, Na Zhang, C. U. I. Xiaolong, **Jiayuan He**, and Ridhi Surana. "Interference-aware scheduling service for virtual GPU enabled systems." U.S. Patent 11,113,093, issued September 7, 2021.

## **AWARDS AND HONORS**

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<i>2<sup>nd</sup> place of ICCAD 2019 Cadthlon Programming Contest</i>	<i>2019</i>
<i>Calhoun Fellowship</i>	<i>2014-2017</i>
<i>Outstanding Graduate</i>	<i>2014</i>
<i>Hengda Scholarship</i>	<i>2013</i>
<i>National Scholarship</i>	<i>2012</i>
<i>Tongfang Scholarship</i>	<i>2010</i>

## **TECHNICAL SKILLS**

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C\C++, CUDA, Verilog, Python